Remarks

This RCE is being filed in response to the Advisory Action dated January 16, 2004. Upon entry of the foregoing amendment, claims 17-33 are pending in the application, with 17, 24, 28, 32, and 33 being the independent claims. Claims 1, 4-12, and 14-16 are sought to be canceled without prejudice to or disclaimer of the subject matter therein. New claims 17-33 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. §§ 102 and 103

Claims 1, 4, 7, and 8 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,317,820 to Shiell et al. (hereinafter "Shiell"). Claims 5, 6, 9-12, and 14-16 were rejected under 35 U.S.C. § 103(a) as being obvious over Shiell in view of U.S. Patent No. 5,761,470 to Yoshida (hereinafter "Yoshida"). Applicant notes that claims 1-16 have been canceled. However, the rejections will be analyzed in light of the new claims.

Independent claim 17 recites:

> A system to process instruction sequences *all having the same predetermined sequence bit length*, the system comprising:
>
> a decode unit to decode an instruction of an instruction sequence received during an instruction fetch, wherein all instructions of the instruction sequence have the same predetermined instruction bit length; and
>
> first and second processing channels, each processing channel including a plurality of functional units, at least one of the functional units of each processing channel being a data processing unit and at least one other of the functional units of each processing channel being a memory access unit;

wherein the decode unit is *operable to determine whether the instruction defines a single operation or two independent operations and to control the first and second processing channels based on the determination.*

Shiell describes a very long word data processor that can be selectively operable in either a first mode or a second mode. In the first mode, the data processor fetches N bits of instructions from the program memory each cycle corresponding to a first program counter. In the second mode, the data processor fetches either N bits of instructions for alternate program counters on alternate cycles, or N/2 bits of instructions corresponding to the first program counter and N/2 bits of instructions corresponding to the second program counter. (Shiell, col. 3, lines 5-15).

The Examiner relies on col. 2, lines 23-56 of Shiell to allegedly show that Shiell teaches a decode unit that is operable to detect for each instruction having a predetermined bit length whether the instruction defines a single operation or two independent operations and to control the first and second channels in dependence on the detection. Applicant, however, contends that the cited art merely shows that, in the second mode, the data processor can process two independent program instruction streams simultaneously. (Shiell, col. 2, lines 43-44). In other words, two instruction *sequences* can be processed simultaneously. Shiell does not even suggest that an instruction within the instruction sequence can include more than one operation. Moreover, Shiell does not suggest that the instruction stream has a predetermined bit length.

More specifically, Shiell fails to teach or suggest a system to process instruction sequences *all having the same predetermined sequence bit length*, wherein the system includes a decode unit that is *operable to determine whether an instruction of the*

instruction sequence defines a single operation or two independent operations and to control the first and second processing channels based on the determination.

Yoshida fails to remedy the failure of Shiell to teach or suggest a system to process instruction sequences *all having the same predetermined sequence bit length*, wherein the system includes a decode unit that is *operable to determine whether an instruction of the instruction sequence defines a single operation or two independent operations and to control the first and second processing channels based on the determination.*

Independent claims 24, 28, 32, and 33 also distinguish over Shiell and Yoshida for reasons similar to those set forth above with respect to independent claim 17, and further in view of their own features. Furthermore, claims 18-23, which depend from claim 17, claims 25-27, which depend from claim 24, and claims 29-31, which depend from claim 28, are also patentable over Shiell and Yoshida, alone or in combination, for at least these reasons, and further in view of their own features. Therefore, Applicant respectfully requests that these rejections be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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